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EXAMINER	
SUGENT, JAMES F	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 08/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,319	HUANG ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-11, 13-15 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/7/2006 and 6/10/2006
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received June 16, 2006 for application number 10/727319 originally filed December 3, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-20 are entered for examination wherein claims 2, 12, 16 and 17 have been cancelled.

The amendment to claim 15 for a claim objection for lack of antecedent basis has been overcome.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 3, 10 and 11 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 8-10, 16 and 18-19 of

copending Application No. 10/727320 (hereinafter referred to as '320) in view of Faucher et al. (U.S. Patent No. 5,404,543) (hereinafter referred to as Faucher). Although the conflicting claims are not identical, they are not patentably distinct from each other because:

In re claim 1, claim 16 of co-pending application '320 meets all the limitations of claim 1 of the instant application except, co-pending application '320 does not explicitly claim the invention further comprising: an output port coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller; and an input port coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller.

Faucher teaches a memory controller (20) that comprises usage evaluator(s) (power management machine 66) that comprise: an output port (access point ["computer interfaces," see below] at which the usage evaluator sends data outside of the memory controller to a programmable memory power system [24]) coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller (Faucher discloses information about the state of all of the memory banks stored within the usage evaluators [power management machine 66] to be used for memory management which are updated to include power saving data that is used outside of memory controller [20] and stored external to the memory controller within a programmable memory power system [24]; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57); and an input port

(access point ["computer interfaces," see below] at which the usage evaluator receives data from outside of the memory controller from memory banks) coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller (Faucher discloses information about the state of all of the memory banks being restored within the usage evaluators [power management machine 66] that are restored by information retrieved from the memory banks themselves outside of the memory controller; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57) (Faucher further discloses the memory controller [20] comprising a computer interface and therefore input and output ports to communicate outside of the controller; column 2, lines 16-24). Faucher has the additional benefit of reducing power within the system memory (column 1, lines 39-49).

It would have been obvious to one of ordinary skill of the art having the teachings of the '320 and Faucher at the time the invention was made, to modify the memory controller of claim 1 of '320 to include input and output ports coupled to the usage evaluators as taught by Faucher. One of ordinary skill in the art would be motivated to make this combination of including input and output ports coupled to the usage evaluators in view of the teachings of Faucher, as doing so would give the added benefit of reducing power consumption within the system memory (as taught by Faucher above).

Claim 3 of the instant invention is identical to claim 18 of '320.

Re claim 10, claim 8 of co-pending application '320 meets all of the limitations of claim 10 of the instant application except co-pending application '320 does not explicitly claim the

invention wherein said device controller further includes: an output port coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator by said processor, whereby a state of said at least one usage evaluator may be stored in said memory by said processor; and an input port coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator by said processor, whereby said state of said at least one usage evaluator may be restored from said memory.

Faucher teaches a memory controller (20) that comprises usage evaluator(s) (power management machine 66) that comprise: an output port (access point ["computer interfaces," see below] at which the usage evaluator sends data outside of the memory controller to a programmable memory power system [24]) coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller (Faucher discloses information about the state of all of the memory banks stored within the usage evaluators [power management machine 66] to be used for memory management which are updated to include power saving data that is used outside of memory controller [20] and stored external to the memory controller within a programmable memory power system [24]; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57); and an input port (access point ["computer interfaces," see below] at which the usage evaluator receives data from outside of the memory controller from memory banks) coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller (Faucher discloses information about the state of all of the memory banks being restored within

the usage evaluators [power management machine 66] that are restored by information retrieved from the memory banks themselves outside of the memory controller; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57) (Faucher further discloses the memory controller [20] comprising a computer interface and therefore input and output ports to communicate outside of the controller; column 2, lines 16-24). Faucher has the additional benefit of reducing power within the system memory (column 1, lines 39-49).

It would have been obvious to one of ordinary skill of the art having the teachings of the '320 and Faucher at the time the invention was made, to modify the memory controller of claim 8 of co-pending application '320 to include input and output ports coupled to the usage evaluators as taught by Faucher. One of ordinary skill in the art would be motivated to make this combination of including input and output ports coupled to the usage evaluators in view of the teachings of Faucher, as doing so would give the added benefit of reducing power consumption within the system memory (as taught by Faucher above).

Claim 11 of the instant invention is identical to claim 9 of '320.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-11, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Faucher et al. (U.S. Patent No. 5,404,543) (hereinafter referred to as Faucher).

As to claim 1, Faucher discloses a device controller (memory controller 20) for coupling (via bus 42) one or more controlled devices (memory modules 30 of memory bank 22) to one or more processors (system CPU 12 and main CPU machine 54) in a processing system (column 3, lines 33-42 and column 3, line 51 thru column 4, line 3 and column 4, lines 25-57), comprising: a command unit (system memory machine 60) for sending commands (RAS and CAS) to said one or more devices (via control bus 36; column 4, lines 25-40 and column 5, lines 54-66); at least one usage evaluator (power management machine 66) having an input coupled (via control bus 36) to an output of said command unit (60) for evaluating a frequency of use of an associated controlled device (Faucher discloses the power management machine [66] comprising counters [one associated for every memory module 30] to establish the "length of time" [hence frequency], since a memory module [30] was used; column 7, lines 38-58); and control logic (power management machine 66) coupled to said usage evaluator (The power management machine [66] and power management scoreboard [64] disclosed by Faucher comprises the functionality listed for both said usage evaluators and control logic as state above) and further coupled to an input of said command unit (Faucher discloses the command unit [system memory machine 60] accommodating various cycles in correlation with control logic [power management machine 66] which necessitates the coupling of these two to each other; column 5, lines 56-61) for sending power management commands in response to said usage evaluator detecting is that a usage level of said associated device has fallen below a threshold level (pre-established time period), whereby said device controller power manages (alters voltage delivered to memory

modules [30]) said controlled device without intervention by said one or more processors (Faucher discloses a power saving method wherein if a memory module [30] has not been accessed within said pre-determined time period then the device controller [memory controller 20] and control logic [power management machine 66] place the memory bank [22] into a lower power mode; column 12, line 67 thru column 13, line 6 and column 13, line 67 thru column 14, line 21) (Though Faucher does not explicitly recite the power managing mode altered in relation to a usage level falling below a threshold, it is well known that if the time since the last access to a device has increased then the frequency of usage has decreased. Hence, if the time period since last access has increased, then frequency of usage has decreased wherein if the frequency of usage has fallen below a threshold [pre-determined time period] then the voltage level to that memory module will be placed into a lower power mode by decreasing the voltage level to the memory module); an output port (access point ["computer interfaces," see below] at which the usage evaluator sends data outside of the memory controller to a programmable memory power system [24]) coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller (Faucher discloses information about the state of all of the memory banks stored within the usage evaluators [power management machine 66] to be used for memory management which are updated to include power saving data that is used outside of memory controller [20] and stored external to the memory controller within a programmable memory power system [24]; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57); and an input port (access point ["computer interfaces," see below] at which the usage evaluator receives data from outside of the memory

controller from memory banks) coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller (Faucher discloses information about the state of all of the memory banks being restored within the usage evaluators [power management machine 66] that are restored by information retrieved from the memory banks themselves outside of the memory controller; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57) (Faucher further discloses the memory controller [20] comprising a computer interface and therefore input and output ports to communicate outside of the controller; column 2, lines 16-24).

As to claim 3, Faucher discloses the device controller wherein said device controller is a memory controller, and wherein said controlled devices are memory modules (column 3, lines 33-42 and column 4, lines 51-55 and column 4, lines 25-40).

As to claim 4, Faucher discloses the device controller wherein said at least one usage evaluator comprises an inter-arrival time counter for determining an interval between accesses to said associated memory module (column 7, lines 38-58).

As to claim 5, Faucher discloses the device controller further comprising one or more power management control registers (70, 72 and 74), each associated with a particular one of said one or more controlled devices (column 6, lines 10-55 and column 7, lines 3-16), each coupled to an input port of said device controller and further coupled to said command unit, whereby a power management control state for said associated controlled device can be set by said one or more processors (54) and set in said associated controlled device by said device controller (column 5, lines 13-24).

As to claim 6, Faucher discloses the device controller wherein said power management control registers are further coupled to said at least one usage evaluator, whereby values of said power management control registers are adjusted in conformity with a result of said evaluating (steps 108, 116, 120, 128 and 134 in figures 5 and 6 reveal the scoreboard [54] being updated after changes made).

As to claim 7, Faucher discloses the device controller wherein said evaluator further comprises an adaptive threshold circuit for adjusting said threshold in response to said evaluated frequency of use of said one or more controlled devices (Faucher discloses changing a threshold [time-out value] dependent on whether system is operating on AC or DC power; column 6, lines 48-55).

As to claim 8, Faucher discloses the device controller wherein said one or more controlled devices include a counter for determining a level of usage of each controlled device during a current process, and wherein said device controller further comprises another input port coupled to each of said controlled devices for reading a value of said counter, and wherein said control logic updates said at associated evaluator in conformity with said value of said counter (column 7, lines 38-58).

As to claim 9, Faucher discloses the device controller wherein said device controller is a memory controller, wherein said controlled devices are memory modules (column 3, lines 33-42 and column 4, lines 51-55 and column 4, lines 25-40) incorporating usage counters (column 7, lines 41-45), and wherein said control logic is coupled to said command logic whereby said control logic periodically reads current counts from said memory modules (column 4, lines 25-57).

As to claim 10, Faucher discloses a processing system (10), comprising: a processor (system CPU 12 and main CPU machine 54); a memory (memory bank 22 consisting of memory modules 30) coupled to said processor for storing program instructions and data values (column 3, lines 33-42 and column 4, lines 25-40); a device controller (memory controller 20) coupled to said processor (column 3, lines 33-50); one or more controlled devices (memory modules 30 within memory bank 22) coupled to said device controller (via buses 32, 34 and 36; column 4, lines 25-40), wherein said controlled devices (memory modules 30) have multiple power management states (column 1, lines 39-49), and wherein said device controller (memory controller 20) includes a command unit (system memory machine 60) for sending commands (RAS and CAS) to said one or more devices (via control bus 36; column 4, lines 25-40 and column 5, lines 54-66), at least one usage evaluator (power management machine 66) having an input coupled (via control bus 36) to an output of said command unit for evaluating a frequency of use of an associated controlled device (column 7, lines 38-58), and control logic (power management machine 66) coupled to said usage evaluator (The power management machine [66] and power management scoreboard [64] disclosed by Faucher comprises the functionality listed for both said usage evaluators and control logic as state above) and further coupled to an input of said command unit (Faucher discloses the command unit [system memory machine 60] accommodating various cycles in correlation with control logic [power management machine 66] which necessitates the coupling of these two to each other; column 5, lines 56-61) for sending power management commands in response to said usage evaluator detecting that a usage level of said associated device has fallen below a threshold level (pre-established time period), whereby said device controller power manages said controlled device without intervention by said

processor (Faucher discloses a power saving method wherein if a memory module [30] has not been accessed within said pre-determined time period then the device controller [memory controller 20] and control logic [power management machine 66] place the memory bank [22] into a lower power mode; column 12, line 67 thru column 13, line 6 and column 13, line 67 thru column 14, line 21) (Though Faucher does not explicitly recite the power managing mode altered in relation to a usage level falling below a threshold, it is well known that if the time since the last access to a device has increased then the frequency of usage has decreased. Hence, if the time period since last access has increased, then frequency of usage has decreased wherein if the frequency of usage has fallen below a threshold [pre-determined time period] then the voltage level to that memory module will be placed into a lower power mode by decreasing the voltage level to the memory module); and wherein said device controller further includes an output port (access point ["computer interfaces," see below] at which the usage evaluator sends data outside of the memory controller to a programmable memory power system [24]) coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator by said processor, whereby a state of said at least one usage evaluator may be stored in said memory by said processor (Faucher discloses information about the state of all of the memory banks stored within the usage evaluators [power management machine 66] to be used for memory management which are updated to include power saving data that is used outside of memory controller [20] and stored external to the memory controller within a programmable memory power system [24]; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57); and an input port (access point ["computer interfaces," see below] at which the usage evaluator receives data from outside of the memory

controller from memory banks) coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator by said processor, whereby said state of said at least one usage evaluator may be restored from said memory (Faucher discloses information about the state of all of the memory banks being restored within the usage evaluators [power management machine 66] that are restored by information retrieved from the memory banks themselves outside of the memory controller; column 4, lines 25-57 and column 6, lines 10-20 and column 6, line 56 thru column 7, line 16 and column 7, lines 38-57) (Faucher further discloses the memory controller [20] comprising a computer interface and therefore input and output ports to communicate outside of the controller; column 2, lines 16-24).

As to claim 11, Faucher discloses the processing system wherein said device controller is a memory controller, and wherein said controlled devices are memory modules (column 3, lines 33-42 and column 4, lines 51-55 and column 4, lines 25-40).

As to claim 13, Faucher discloses the processing system wherein said at least one usage evaluator comprises an inter-arrival time counter for determining an interval between commands sent to said associated controlled device (column 7, lines 38-58).

As to claim 14, Faucher discloses the processing system wherein said device controller further comprises one or more power management control registers (70, 72 and 74), each associated with a particular one of said one or more controlled devices (column 6, lines 10-55 and column 7, lines 3-16), each coupled to an input port of said device controller and further coupled to said command unit, whereby a power management control state for said associated controlled device can be set by said processor (54) and set in said associated controlled device by said device controller (column 5, lines 13-24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 15 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faucher (as cited above) in view of Fleck et al. (U.S. Patent No. 6,128,641) (hereinafter referred to as Fleck).

As to claim 15, Faucher discloses a method of managing power in a processing system (column 1, lines 39-49), comprising: sending power management setting information for devices (memory modules 30 of memory bank 22) controlled by a device controller (memory controller 20) to said device controller (column 4, lines 25-57); evaluating a usage (track length of time since last access via counters) of each of said controlled devices (memory modules 30 of memory bank 22) within said device controller (via power management machine [66] found within memory controller [20]) in order to determine whether or not said usage has fallen below

a threshold (Though Faucher does not explicitly recite the power managing mode altered in relation to a frequency falling below a threshold, it is well known that if the time since the last access to a device has increased then the frequency of usage has decreased. Hence, if the time period since last access has increased, then frequency of usage has decreased wherein if the frequency of usage has fallen below a threshold [pre-determined time period] then the voltage level to that memory module will be placed into a lower power mode by decreasing the voltage level to the memory module; column 7, lines 38-58 and column 13, line 67 thru column 14, line 21); sending power management commands ("number of inputs from memory controller") from said device controller to said controlled devices (via programmable memory power system [24]; column 3, line 51 thru column 4, line 3) in conformity with a result of said determining, whereby said device controller manages a power management state of said controlled devices without processor intervention (Faucher discloses a power saving method wherein if a memory module [30] has not been accessed within said pre-determined time period then the device controller [memory controller 20] and control logic [power management machine 66] place the memory bank [22] into a lower power mode; column 12, line 67 thru column 13, line 6 and column 13, line 67 thru column 14, line 21).

Faucher does not explicitly disclose receiving an indication of a context switch activating a second process and deactivating a first process; and in response to said receiving, saving a state of said evaluating, whereby said state may be restored at a subsequent context switch receiving an indication of a context switch activating a second process and deactivating a first process; and in response to said receiving, saving a state of said evaluating, whereby said state may be restored at a subsequent context switch.

Fleck teaches a data processing unit that comprises register file (2), system memory (1) and an instruction control unit (3) to assist in context switching. Fleck further teaches receiving an indication of a context switch activating a second process and deactivating a first process; and in response to said receiving, saving a state of said evaluating, whereby said state may be restored at a subsequent context switch receiving an indication of a context switch activating a second process and deactivating a first process; and in response to said receiving, saving a state of said evaluating, whereby said state may be restored at a subsequent context switch (Fleck teaches a first context state being preserved in memory when second context state is initiated. Fleck further teaches the first context state being restored once the second context state is completed; column 1, line 45 thru column 2, line 45). Fleck has the additional feature of decreasing memory space needed and reducing execution overhead (column 1, lines 28-35).

It would have been obvious to one of ordinary skill of the art having the teachings of Faucher and Fleck at the time the invention was made, to modify the power managing method of Faucher to include saving and recovering context switch states as taught by Fleck. One of ordinary skill in the art would be motivated to make this combination of include saving and recovering context switch states in view of the teachings of Fleck, as doing so would give the added benefit of decreasing memory space needed and reducing execution overhead (as taught by Fleck above).

As to claim 18, Faucher in combination with Fleck taught the power managing method in claim 15, as shown above. Fleck further teaches the method further comprising retrieving usage counts from said controlled devices, and wherein said evaluating is performed in conformity with said retrieved usage counts (column 3, line 56 thru column 4, line 5).

As to claim 19, Faucher in combination with Fleck taught the power managing method in claim 15, as shown above. Faucher further teaches the method further comprising adjusting said threshold in accordance with a result of said evaluating, whereby said evaluating is made adaptive to said usage (Faucher discloses changing a threshold [time-out value] dependent on whether system is operating on AC or DC power; column 6, lines 48-55).

As to claim 20, Faucher in combination with Fleck taught the power managing method in claim 15, as shown above. Faucher further teaches the method wherein said device controller is a memory controller, wherein said controlled devices are memory modules (column 3, lines 33-42 and column 4, lines 51-55 and column 4, lines 25-40), wherein said sending sends power management setting information to said memory modules, and wherein said evaluating determines a frequency of accesses to said memory modules (column 7, lines 41-45) (Faucher discloses a power saving method wherein if a memory module [30] has not been accessed within said pre-determined time period then the device controller [memory controller 20] and control logic [power management machine 66] place the memory bank [22] into a lower power mode; column 12, line 67 thru column 13, line 6 and column 13, line 67 thru column 14, line 21) (Though Faucher does not explicitly recite the power managing mode altered in relation to a usage level falling below a threshold, it is well known that if the time since the last access to a device has increased then the frequency of usage has decreased. Hence, if the time period since last access has increased, then frequency of usage has decreased wherein if the frequency of usage has fallen below a threshold [pre-determined time period] then the voltage level to that memory module will be placed into a lower power mode by decreasing the voltage level to the memory module).

Response to Arguments

Applicant's arguments with respect to claims 1, 3-11, 13-15 and 18-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or (571) 272-1000.

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August 9, 2006

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